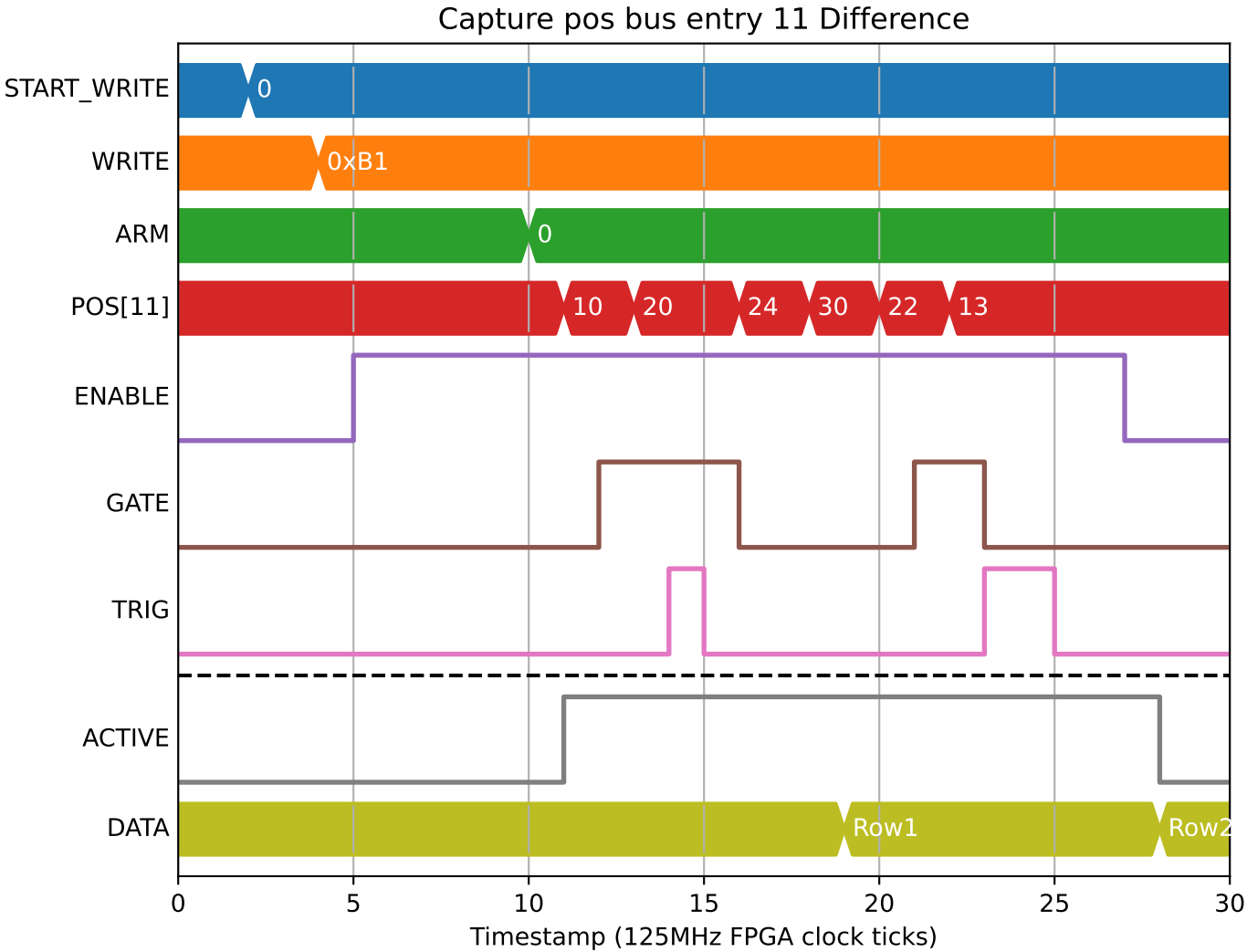
Capture pos bus entry 11 Difference
START_WRITE
0
WRITE
0xB1
ARM
0
POS[11]
10
20
24
30
22
13
ENABLE
GATE
TRIG
ACTIVE
DATA
Row1
Row2
0
5
10
15
20
25
30
Timestamp (125MHz FPGA clock ticks)