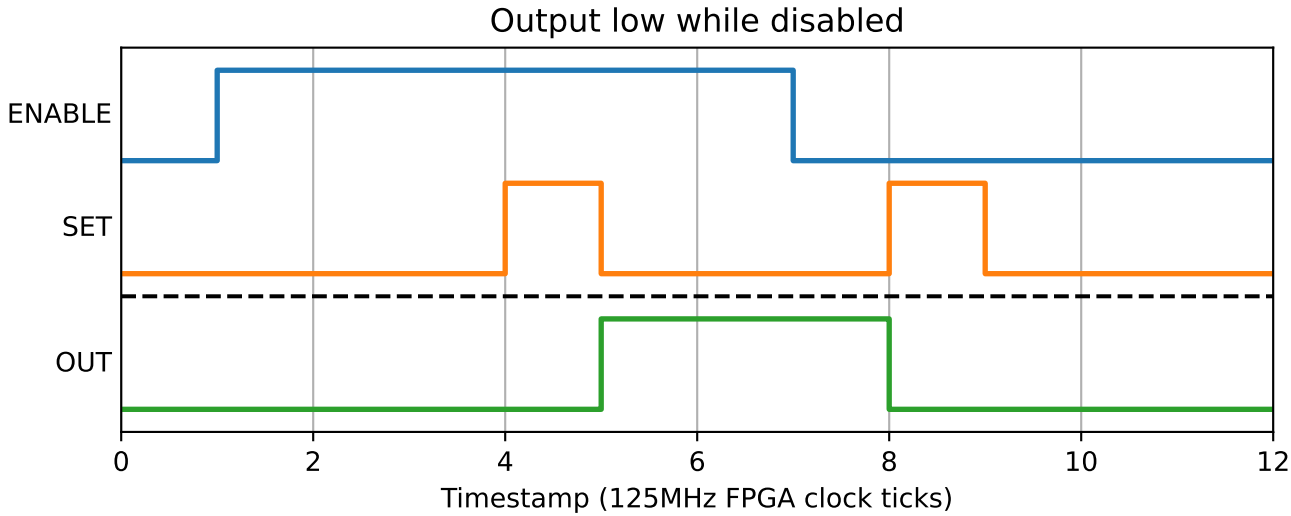
Output low while disabled
ENABLE
SET
OUT
0
2
4
6
8
10
12
Timestamp (125MHz FPGA clock ticks)