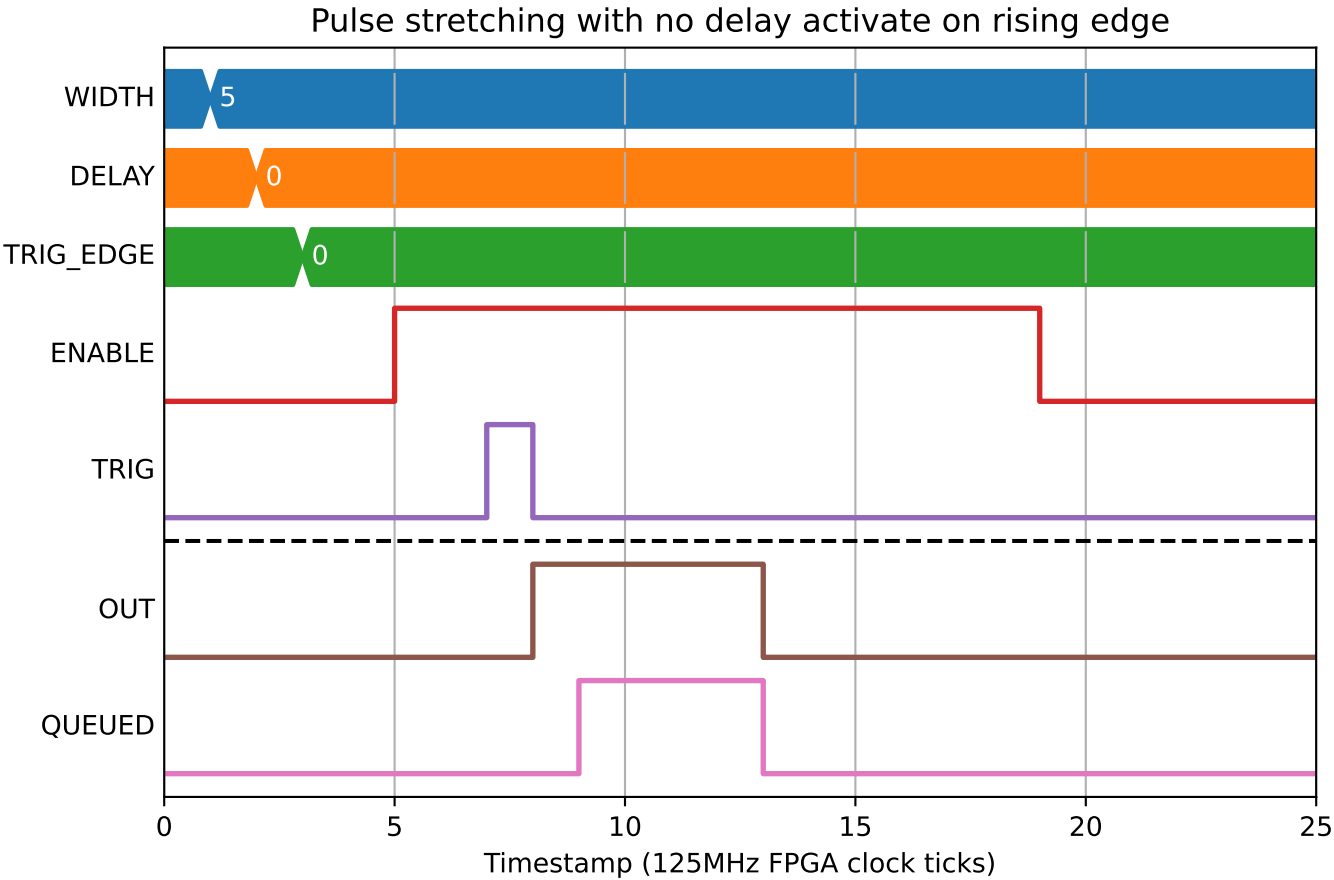
Pulse stretching with no delay activate on rising edge
WIDTH
5
DELAY
0
TRIG_EDGE
0
ENABLE
TRIG
OUT
QUEUED
0
5
10
15
20
25
Timestamp (125MHz FPGA clock ticks)